WHAT IS CLAIMED IS:

1. A magnetic random access memory comprising:

a plurality of cell units each of which comprises cross-point memory cells that exhibit a magnetoresistive effect;

word lines each of which is connected to one terminal of a corresponding one of the memory cells in each cell unit;

sub bit lines each of which is commonly connected to the other terminal of each of the plurality of memory cells as a predetermined unit in each cell unit;

main bit lines which are commonly connected to said plurality of sub bit lines through switch circuits, respectively, and form a hierarchical bit line structure together with the sub bit lines;

a column select circuit configured to select the main bit line and connect the main bit line to a sense amplifier; and

a row select circuit configured to select the word line for each cell unit by controlling the switch circuits, and in read operation, set, in a floating state, the word lines except the selected word line with a selected memory cell connected, to which unselected memory cells connected to the sub bit line to which the selected memory cell is connected are connected, and set the word lines connected to the memory cells in the cell unit which does not include

the selected memory cell to the same potential as that of the main bit line.

2. The memory according to claim 1, wherein the cell unit is a memory cell block in which the memory cells are laid out in a matrix, one terminal of each of the memory cells in each memory cell block is connected to a corresponding one of the word lines for each row, and the other terminal is connected to a corresponding one of the sub bit lines for each column.

3. The memory according to claim 1, wherein the switch circuit includes a first MOS transistor which has a current path whose one end is connected to the sub bit line and whose other end is connected to the main bit line for each column, and which is ON/OFF-controlled by a cell unit select signal output from the row select circuit.

4. The memory according to claim 1, wherein the column select circuit comprises a second MOS transistor for column selection, which has a current path whose one terminal is connected to the main bit line and whose other terminal is connected to the sense amplifier, a column select line which is connected to a gate of the second MOS transistor, a CSL driver which outputs a column address select signal to the column select line to selectively drive the column select line, a column decoder which decodes a column address signal and supplies the column address signal to

the CSL driver, and a first bias circuit which selectively applies a bias voltage to the main bit line on the basis of the column address select signal output from the CSL driver.

5. The memory according to claim 1, wherein the row select circuit includes a read word line driver which selectively drives the word line for each cell unit and controls the switch circuit for each cell unit to connect the sub bit line in the cell unit which includes the selected memory cell to the main bit line, and a row decoder which decodes a row address signal and supplies the row address signal to the read word line driver.

6. The memory according to claim 1, wherein the row select circuit includes a third MOS transistor which has a current path whose one end is connected to one end of the word line and whose other end is commonly connected, a second bias circuit which applies a bias voltage to said other terminal of the third MOS transistor, a first read word line driver which drives the third MOS transistor for each cell unit, a first row decoder which decodes a row address signal and supplies the row address signal to the first read word line driver, a fourth MOS transistor which has a current path whose one end is connected to the other end of the word line and whose other end is commonly connected, a second read word line driver which

selectively drives the fourth MOS transistor and controls the switch circuit for each cell unit to connect the sub bit line in the cell unit which includes the selected memory cell to the main bit line, and a second row decoder which decodes the row address signal and supplies the row address signal to the second read word line driver.

7. The memory according to claim 1, wherein the row select circuit includes a third MOS transistor which has a current path whose one end is connected to one end of the word line and whose other end is commonly connected, a second bias circuit which applies a bias voltage to the other terminal of the third MOS transistor, a fourth MOS transistor which has a current path whose one end is connected to the other end of the word line and whose other end is commonly connected, a read word line driver which selectively drives the fourth MOS transistor and controls the switch circuit and the third MOS transistor for each cell unit to connect the sub bit line in the cell unit which includes the selected memory cell to the main bit line and connect the word line to the second bias circuit, and a row decoder which decodes a row address signal and supplies the row address signal to the read word line driver.

8. The memory according to claim 7, wherein the third MOS transistor comprises an NMOS transistor, and

an inverted signal of the signal supplied to the switch circuit is supplied to a gate of the third MOS transistor for each cell unit.

9. The memory according to claim 7, wherein the third MOS transistor comprises a PMOS transistor, and the signal supplied to the switch circuit is supplied to a gate of the third MOS transistor for each cell unit.

10. The memory according to claim 4, wherein the first bias circuit stops applying the bias voltage to the selected main bit line on the basis of a column address select signal output from the CSL driver.

11. The memory according to claim 10, wherein the selected main bit line is connected to the sense amplifier in response to the column address select signal, and a voltage substantially equal to the bias voltage output from the first bias circuit is applied from the sense amplifier to the selected main bit line.

12. The memory according to claim 6, wherein the bias voltage output from the second bias circuit is substantially equal to the bias voltage output from the first bias circuit.

13. The memory according to claim 7, wherein the bias voltage output from the second bias circuit is substantially equal to the bias voltage output from the first bias circuit.

14. The magnetic random access memory comprising:

a memory cell array of a hierarchical bit line scheme in which cross-point memory cells that exhibit a magnetoresistive effect are laid out in a matrix, and a read bit line to be used in a data read mode is constituted by a main bit line and a sub bit line; and

word line potential setting means for, in read operation, setting, in a floating state, word lines to which unselected memory cells connected to the sub bit line to which the selected memory cell is connected are connected, and setting word lines except the word lines, which are connected to sub bit lines which do not include the selected memory cell to a potential substantially equal to the main bit line.

15. The memory according to claim 14, wherein a potential of the word line connected to the selected memory cell is different from those of the word lines connected to unselected memory cells connected to the sub bit lines which do not include the selected memory cell.

16. The memory according to claim 14, further comprising bias means for holding the potential of the main bit line at a predetermined bias voltage.

17. The memory according to claim 16, wherein the bias means stops applying the bias voltage to the selected main bit line in response to a column address select signal which selects a column address of the memory cell array.

18. The memory according to claim 17, wherein the selected main bit line is connected to a sense amplifier in response to the column address select signal, and a voltage substantially equal to the bias voltage output from the bias means is applied from the sense amplifier to the selected main bit line.

19. A magnetic random access memory comprising:

a memory cell array of a hierarchical bit line scheme in which cross-point memory cells that exhibit a magnetoresistive effect are laid out in a matrix, and a read bit line to be used in a data read mode is constituted by a main bit line and a sub bit line;

connection means for selectively connecting a word line to select the memory cell to one of first and second potential supply sources which are different from each other; and

control means for controlling the connection means to set the word line in an electrical floating state.

20. The memory according to claim 19, wherein

the control means comprises first and second row decoders and word line drivers to set a potential of the word line in the read mode, and

when the connection means is deactivated by the first and second row decoders and word line drivers, the word line is set in the electrically floating state.

21. The memory according to claim 20, wherein

the connection means comprises first and second selection circuits which connect the word line to the first and second potential supply sources on the basis of output signals from the first and second row decoders and word line drivers, each of the first and second selection circuits being constituted by an NMOS transistor, and the MOS transistor is controlled by the output signals from the first and second row decoders and word line drivers.

22. The memory according to claim 21, wherein the signal supplied from the first row decoder and word line driver to the first selection circuit is independent for each sub bit line, and the signal supplied from the second row decoder and word line driver to the second selection circuit is independent for each word line.

23. The memory according to claim 19, wherein

the control means comprises a row decoder and word line driver to set a potential of the word line in the read mode, and

when the connection means is deactivated by the row decoder and word line driver, the word line is set in the electrically floating state.

24. The memory according to claim 23, wherein the connection means comprises first and second selection circuits which connect the word line to the first and second potential supply sources on the basis of

an output signal from the row decoder and word line driver, each of the first and second selection circuits being constituted by an NMOS transistor, and the MOS transistor is controlled by the output signal from the row decoder and word line driver.

25. The memory according to claim 24, wherein the signal supplied from the row decoder and word line driver to the first selection circuit is a signal obtained by logically inverting a select signal between the main bit line and the sub bit line, and the signal supplied from the row decoder and word line driver to the second selection circuit is independent for each word line.

26. The memory according to claim 23, wherein the connection means comprises first and second selection circuits which connect the word line to the first and second potential supply sources on the basis of an output signal from the row decoder and word line driver, the first selection circuit being constituted by a PMOS transistor, and the second selection circuit being constituted by an NMOS transistor, and the MOS transistor is controlled by the output signal from the row decoder and word line driver.

27. The memory according to claim 26, wherein the output signal supplied from the row decoder and word line driver to the first selection circuit is a select signal between the main bit line and the sub bit line,

and the output signal supplied from the row decoder and word line driver to the second selection circuit is independent for each word line.

28. A method of reading data from a magnetic random access memory including a memory cell array of a hierarchical bit line scheme in which cross-point memory cells that exhibit a magnetoresistive effect are laid out in a matrix, and a read bit line to be used in a data read mode is constituted by a main bit line and a sub bit line, comprising:

asserting a word line connected to a memory cell to be selected and setting word lines in a floating state, the word lines being connected to unselected memory cells connected to the sub bit line to which the memory cell to be selected is connected; and

setting word lines except the word lines, which are connected to the sub bit lines which do not include the selected memory cell, to a potential substantially equal to the main bit line.

29. The method according to claim 28, further comprising

after setting the word lines to the potential substantially equal to the main bit line,

connecting the sub bit line to which the selected memory cell is connected to the main bit line and selecting the main bit line and connecting the main bit line to a sense amplifier, and

causing the sense amplifier to detect and amplify stored data in the selected memory cell and read out the data.